



X-1770 US  
09/649,437

PATENT  
Conf. No.: 6896

IN THE UNITED STATES PATENT OFFICE

Applicants: Bart Reynolds et al.  
Assignee: Xilinx, Inc.  
Title: Method and Apparatus for Specifying  
Addressability and Bus Connections in a Logic  
Design  
Serial No.: 09/649,437 File Date: 08-23-00  
Examiner: Eduardo Garcia Otero Art Unit: 2123  
Docket No.: X-1770 US Conf. No.: 6896

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Technology Center 2100

AMENDMENT IN RESPONSE TO FINAL OFFICE ACTION

Dear Sir:

In response to the Final Office Action mailed from the  
Patent Office on April 22, 2004, please replace/substitute the  
following claims as indicated.

**Amendments to the Claims** are reflected in the listing of claims  
which begins on page 2 of this paper.

**Remarks/Arguments** begin on page 8 of this paper.